

REMARKS

Examiner Dang is thanked for his thorough examination of the Subject Patent Application. Regarding the rejection of 1 - 6, 9 - 12, and 14, under 35 USC 103(a) as being unpatentable over Bai et al, in view of Despande et al, it should be noted that applicants previously amended Claim 1, clearly states that an amorphous silicon layer is deposited **directly** on the underlying conductive layer, **wherein this same underlying conductive layer directly overlays the gate insulator layer**. In the Bai prior art silicon layer 208 which is consumed to form metal silicide, overlays barrier layer 206, which in turn overlays silicon layer 204, which interfaces gate insulator layer 202. This major process difference results in a Bai process wherein a silicon shape is formed on an oxide or barrier layer 206, which in turn overlays a conductive shape, with the oxide or barrier shape remaining as a component of the Bai invention. The Bai art probably needed the oxide layer as a barrier to prevent consumption of the conductive layer during silicide formation wherein applicant's unique process featured consumption of an amorphous silicon shape directly on an underlying conductive shape without the use of an insulator or barrier layer, without risk to, or consumption of underlying conductive material. The Despande, Wu, and Wieczorek prior art only describe process details similar to applicants's however no combination of the cited prior art can result in applicant's unique process sequence in which an amorphous silicon shape, formed **directly** on the underlying conductive shape which in turn directly interfaces the underlying gate insulator. The major process feature, not including a layer between an overlying amorphous silicon layer and an

IME03-011C

underlying conductive layer on a gate insulator layer, **without the use of a intervening barrier or oxide layer**, results in a less complex and cheaper process than the process described in the Bai invention. Applicant's process described in previously amended independent Claims 1 and 16, featuring a metal silicide shape formed **directly** on the underlying conductive shape which in turn directly overlays a gate insulator layer, is novel and different the Bai process which describes the use of an intervening barrier or oxide layer between the metal silicide shape and the conductive shape which in turn interfaces the gate insulator layer. Therefore reconsideration of independent Claims 1 as well as referencing dependent Claims is requested.

The same argument, formation of an amorphous silicon layer or shape, **directly** on an underlying conductive layer which in turn directly interfaces a gate insulator layer, **without the use of underlying insulator barrier layer** as shown in the Bai prior art, is used to argue the rejection of Claims 16 - 21, 24 - 28, and 31, under 35 USC 103 (a) as being unpatentable Bai taken with Despande, in further view of Wieczorek. Again the critical feature of forming amorphous material directly on the conductive material which in turn directly interfaces the gate insulator layer, without intervening barrier material, is only shown in applicant's process not in any of, or in a combination of, cited prior art. Again the Bai prior art shows the silicon layer which is used for metal silicide formation, interfacing a barrier layer 206, unlike applicants process in which the silicon layer used for metal silicide formation overlays the conductive layer which directly overlays the gate insulator layer. Therefore reconsideration of the rejection of independent Claim 16, and dependent Claims 17 - 21, and 24 - 28, referencing a unique

IME03-011C

independent Claim 16, is requested.

Regarding the rejection of independent Claims 1 and 16, under 35 USC 103(a), as being unpatentable over Chau et al (US 5,625,217 B1), in view of Nguyen et al (US 6,084,279), taken with Bai et al, Despande et al, in view of Wieczorek, again no combination features **an amorphous silicon shape formed directly on the underlying conductive shape which in turn directly overlays a gate insulator layer, wherein an amorphous silicon layer used to form the amorphous silicon shape is totally consumed during silicide formation.** It is obvious the Chau prior art does not totally consume the amorphous silicon layer overlying a conductive layer, therefore only forming metal silicide on an unconsumed portion of the amorphous silicon layer. Therefore the Chau prior art will not result in the low gate resistance and no polysilicon depletion obtained via applicants process in which all high resistance material is consumed during the silicidation procedure. Therefore it is strongly believed that the Chau prior art in combination with the above referencing prior art, do not lead to a process sequence in which an amorphous silicon shape, formed directly on an underlying conductive shape, (precluding the use of a insulator barrier layer), is totally consumed during the formation of an metal silicide region directly on an underlying conductive shape. Therefore reconsideration of independent Claims 1 and 16, as well as all non-cancelled dependent referencing independent Claims 1 and 16 is requested.

Again the essence of applicant's process (invention) is the formation of a metal silicide shape (via **total** consumption of an amorphous silicon layer) on an underlying conductive layer or


IME03-011C

shape, wherein this underlying conductive layer or shape is located directly on an underlying gate insulator layer. Prior art cited by Examiner describes a metal silicide layer formed **not directly** on the conductive layer or shape which interfaces the gate insulator layer. It is believed this major difference clearly puts applicant's invention in condition for allowance.

Dependent Claims 13, and 29 - 30, have previously been cancelled.

Allowance of all Claims (1- 12, 14 - 28, 31) is requested.

It is requested that should Examiner Dang not find that the Claims are now Allowable that he call the undersigned attorney at 845-452-5863, to overcome any problems preventing allowance.

Respectfully submitted,

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